WHAT IS CLAIMED IS:

1.   An automatic frequency control signal generating circuit comprising:

a first frequency error detection unit for extracting from an input signal at least two known different symbols as a first symbol set, detecting a frequency error of said input signal on the basis of said extracted first symbol set and delivering said frequency error;

a second frequency error detection unit for extracting from said input signal at least two known symbols having a symbol distance different from that of said first symbol set as a second symbol set, detecting a frequency error of said input signal on the basis of said extracted second symbol set and delivering said frequency error;

a decision unit for deciding which one of the outputs of said first and second frequency error detection units is selected; and

a control signal unit for generating a control signal adapted to control the frequency of said input signal on the basis of the output of frequency error detection unit selected by said decision unit.

2.   An automatic frequency control signal generating circuit according to claim 1, wherein said control signal unit includes:

a positive/negative decision unit for deciding whether the output of any one of said first

and second frequency error detection units selected by said decision unit is a positive value or a negative value and delivering a result of decision; and

an accumulating unit for accumulating the value delivered out of said positive/negative decision unit and delivering an integrated signal as said control signal.

3.   An automatic frequency control signal generating circuit according to claim 2, wherein said decision unit compares a predetermined reference value with absolute values of the respective output values of said first and second frequency error detection units and selects an output of any one of said first and second frequency error detection units in accordance with a comparison result.

4.   An automatic frequency control signal generating circuit according to claim 3, wherein a frame format of said input signal includes a known pilot signal, a data area of predetermined symbol length and a known synchronous word symbol area of predetermined symbol length, said first frequency error detection unit extracts at least two synchronous word symbols in said synchronous word symbol area, and said second frequency error detection unit extracts said pilot signal and a synchronous word symbol in said synchronous word symbol area.

5.   An automatic frequency control signal generating circuit according to claim 1, wherein said

first frequency error detection unit includes:

a first multiplier for calculating and delivering a product of one symbol of said first symbol set and a complex conjugate of said symbol;

a first phase inverter for inverting and delivering the phase of the value delivered out of said first multiplier;

a second multiplier for calculating and delivering a product of another symbol of said first symbol set and a complex conjugate of said symbol;

a third multiplier for performing complex multiplication of the output of said phase inverter and the value delivered out of said second multiplier and delivering a complex product; and

a first phase detection unit for detecting the phase of the output of said third multiplier and delivering said detected phase as said frequency error, and wherein

said second frequency error detection unit includes:

a fourth multiplier for calculating and delivering a product of one symbol of said second symbol set and a complex conjugate of said symbol;

a second phase inverter for inverting and delivering the phase of the value delivered out of said fourth multiplier;

a fifth complex multiplier for calculating and delivering a product of another symbol of said

second symbol set and a complex conjugate of said
symbol;

a sixth multiplier for performing complex
multiplication of the output of said phase inverter and
the value delivered out of said fifth complex
multiplier and delivering a complex product; and

a second phase detection unit for detecting
the phase of the output of said sixth complex
multiplier and delivering said detected phase as said
frequency error.

6.   An automatic frequency control signal
generating circuit according to claim 5, wherein one
symbol of said first symbol set inputted to said first
multiplier and another symbol of said first symbol set
inputted to said second multiplier are located at
positions which are distant from each other by n
symbols in said input signal, where n is the power of
2.

7.   An automatic frequency control signal
generating circuit according to claim 5, wherein the
frame format of said input signal includes a data area
of predetermined symbol length and a known synchronous
word symbol area of predetermined symbol length, one
symbol of said first symbol set inputted to said first
multiplier is an initial synchronous word symbol of
said synchronous word symbol area, another symbol of
said first symbol set inputted to said second
multiplier is one synchronous word symbol selected from

a second and ensuing synchronous word symbols of said synchronous word symbol area, and said first frequency error detection unit further includes a switch unit for selecting and delivering one desired synchronous word symbol from the second and ensuing synchronous word symbols of said synchronous word symbol area of said input signal.

8.   An automatic frequency control signal generating circuit according to claim 7, wherein one symbol to be selected from the second and ensuing synchronous word symbols by means of said switch unit is located at a position which is distant from said initial synchronous word symbol by n symbols, where n is the power of 2.

9.   An apparatus for receiving signals having the automatic frequency control signal generating circuit as recited in claim 1, further comprising:

an RF receiving circuit for performing frequency conversion of a received signal, converting the received signal subjected to the frequency conversion into a digital signal and delivering it;

an oscillator for delivering to said RF receiving circuit a reference frequency signal for the frequency conversion;

a quadrature detector for converting the received signal subjected to the digital conversion into a baseband signal and delivering it;

a filter for eliminating unwanted frequency

components of the received baseband signal and delivering a resulting signal;

a frequency corrector for correcting an error between the frequency of the baseband signal delivered out of said filter and the frequency of said reference frequency signal on the basis of said control signal from said automatic frequency control signal generating circuit and delivering a corrected baseband signal;

a demodulator for demodulating and delivering the baseband signal received from said frequency corrector; and

a buffer for holding the output of said frequency corrector, wherein

said automatic frequency control signal generating circuit extracts said first and second symbol sets from said input signal now represented by the signal held in said buffer and generates said control signal on the basis of said symbol sets to supply said control signal to said frequency corrector.

10. A radio base station apparatus comprising:

the receiving apparatus as recited in claim 9; and

a radio transmitting circuit for converting a signal of baseband zone to be transmitted, which signal is converted to an analog signal, into a signal of radio frequency band on the basis of the reference frequency signal of said oscillator.

11. A radio transmitting/receiving system for

signals comprising:

the radio base station as recited in claim 10; and

at least one mobile radio transmitting/receiving apparatus, wherein

said at least one mobile radio transmitting/receiving apparatus receives a transmitting signal from said radio base station and controls a reference frequency signal inside said mobile radio transmitting/receiving apparatus on the basis of a reference frequency signal extracted from said received signal.

12.   An apparatus for receiving signals having the automatic frequency control signal generating circuit as recited in claim 1, further comprising:

an RF receiving circuit for performing frequency conversion of a received signal, converting the received signal subjected to the frequency conversion into a digital signal and delivering it;

an oscillator for delivering to said RF receiving circuit a reference frequency signal for the frequency conversion;

a quadrature detector for converting the received signal subjected to digital conversion into a baseband signal and delivering it;

a filter for eliminating unwanted frequency components from the received baseband signal and delivering a resulting signal;

a demodulator for demodulating and delivering the baseband signal received from said filter; and

a buffer for holding the output of said frequency corrector, wherein

said automatic frequency control signal generating circuit extracts said first and second symbol sets from said input signal now represented by the signal held in said buffer and generates said control signal on the basis of said symbol sets, and said receiving apparatus further includes a frequency controller for controlling said reference frequency signal of said oscillator on the basis of said control signal from said automatic frequency control signal generating circuit.

13.   A radio terminal apparatus comprising:

the receiving apparatus as recited in claim 12; and

a radio transmitting circuit for converting a signal of baseband zone to be transmitted, which signal is converted into an analog signal, into a signal of radio frequency band on the basis of the reference frequency signal of said oscillator.

14.   A frequency error detection method comprising:

a) a step of extracting at least two known different symbols as a first symbol set from an input signal;

b) a step of calculating and delivering a

product of one symbol of said first symbol set and a complex conjugate of said symbol;

c) a step of inverting and delivering the phase of the output in said step b);

d) a step of calculating and delivering a product of another symbol of said first symbol set and a complex conjugate of said symbol;

e) a step of performing complex multiplication of the outputs in said steps c) and d) and delivering a product; and

f) a step of detecting the phase of the output in said step e) and delivering said detected phase as a first frequency error of said input signal.

15. A frequency error detection method according to claim 14, wherein one symbol of said first symbol set in said step b) and another symbol in said first symbol set in said step d) are located at positions which are distant from each other by n symbols inside said input signal, where n is the power of 2.

16. A frequency error detection method according to claim 14, wherein when the frame format of said input signal includes a data area of predetermined symbol length and a known synchronous word symbol area of predetermined symbol length, one symbol of said first symbol set in said step b) is the initial synchronous word symbol of said synchronous word symbol area and another symbol of said first symbol set in said step d) is one synchronous word symbol desirably

selected from the second and ensuing synchronous word

symbols of said synchronous word symbol area.

17.   A frequency error detection method according

to claim 14 further comprising:

g)   a step of extracting, as a second symbol set,

at least two known symbols having a different symbol

distance form that in said first symbol set from said

input signal;

h)   a step of calculating and delivering a

product of one symbol of said second symbol set and a

complex conjugate of said symbol;

i)   a step of inverting and delivering the phase

of the value delivered in said step h);

j)   a step of calculating and delivering a

product of another symbol of said second symbol set and

a complex conjugate of said symbol;

k)   a step of performing complex multiplication

of the outputs in said steps i) and j) and delivering a

product;

l)   a step of detecting the phase of the output

in said step k) and delivering said detected phase as a

second frequency error of said input signal; and

m)   a step of selecting any one of said first and

second frequency errors on the basis of a predetermined

condition.

18.   A frequency error detection method according

to claim 17, wherein when said first frequency error is

ϕ_1, said second frequency error is ϕ_2 and a positive

reference value preset desirably is ϕ_{th}, said step m) further includes a step of selecting said second frequency error ϕ_2 if an absolute value $|\phi_1|$ of said first frequency error ϕ_1 satisfies $|\phi_1| \leq \phi_{th}$ but selecting said first frequency error ϕ_1 if $|\phi_1|$ satisfies $|\phi_1| > \phi_{th}$.

19.   A method for receiving signals having the steps a) to m) as recited in claim 18, further comprising:

n)   a step of performing frequency conversion of a received signal, converting the received signal subjected to the frequency conversion into a digital signal and delivering it;

o)   a step of delivering a reference frequency signal for said frequency conversion in said step n);

p)   a step of converting the received signal subjected to digital conversion into a baseband signal to cause it to be applied with quadrture detection and then delivered;

q)   a step of eliminating unwanted frequency components from the delivered baseband signal;

r)   a step of correcting an error between the frequency of the baseband signal delivered in said step q) and the frequency of said reference frequency signal on the basis of the frequency error signal delivered in said step m) and delivering the corrected error;

s)   a step of demodulating and delivering the output of the pbaseband signal in said step r); and

wherein

the extraction of said first and second symbol sets in said steps a) and g) is carried out from the signal held in said step t).

20.   A method for transmitting and receiving signals having the steps a) to t) as recited in claim 19, further comprising:

a step of converting a signal of baseband zone to be transmitted, which signal is converted into an analog signal, into a signal of radio frequency band on the basis of said reference frequency signal and transmitting the converted radio frequency band signal.

21.   An automatic frequency control signal generating circuit comprising:

a frequency error detection unit for extracting at least two known different symbols as a first symbol set from an input signal, further extracting, as a second symbol set, at least two known symbols having a different symbol distance from that of said first symbol set from said input signal, detecting first and second frequency errors of said input signal on the basis of said extracted first and second symbol sets and delivering them;

a decision unit for deciding in accordance with the error values which one of the outputs of said first and second frequency errors is selected; and

a control signal unit for generating a control signal adapted to control the frequency of said

input signal on the basis of the first or second
frequency error selected by said decision unit.

22.   An automatic frequency control signal
generating circuit according to claim 21, wherein when
the frame format of said input signal includes a known
pilot signal, a data area of predetermined symbol
length and a known synchronous word symbol area of
predetermined symbol length, said first symbol set
includes said pilot signal and one synchronous word
symbol in the synchronous word symbol area and said
second symbol set includes two synchronous word symbols
in said synchronous word symbol area, wherein said
frequency error detection unit further includes:

a switch unit for selecting and delivering
any one of the pilot signal or one synchronous word
symbol of said synchronous word symbol area in one
frame of said input signal;

a first multiplier for calculating and
delivering a product of the symbol delivered out of
said switch unit and a complex conjugate of said
symbol;

a phase inversion unit for inverting and
delivering the phase of the value delivered out of said
multiplier;

a second multiplier for calculating and
delivering another synchronous word symbol of said
synchronous word symbol area and a complex conjugated
of said symbol;

a third multiplier for performing complex multiplication of the output of said phase inversion unit and the output of said second multiplier and delivering a complex product; and

a phase detection unit for detecting the phase of the output of said third multiplier and delivering the detected phase as said frequency error, and wherein

the phase detected by said phase detection unit when said switch selects said pilot signal is made to be said first frequency error and the phase detected by said phase detection unit when said switch unit selects one synchronous word symbol of said synchronous word symbol area is made to be said second frequency error.